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ABSTRACT

Development of manufacturing infrastructure is required to ensure a commercial source of mask substrates for the timely introduction of EUVL. Improvements to the low thermal expansion materials that compose the substrate have been made, but need to be scaled to production quantities. We have been evaluating three challenging substrate characteristics to determine the state of the infrastructure for the finishing of substrates. First, surface roughness is on track and little risk is associated with achieving the roughness requirement as an independent specification. Second, with new flatness-measuring equipment just coming on line, the vendors are poised for improvement toward the SEMI P37 flatness specification. Third, significant acceleration is needed in the reduction of defect levels on substrates. The lack of high-sensitivity defect metrology at the vendors' sites is limiting progress in developing substrates for EUVL.

Keywords: EUV lithography, EUVL reticles, EUVL substrates, EUVL masks.

1. INTRODUCTION

The ITRS Roadmap for Extreme Ultraviolet Lithography (EUVL)[1] calls for substantial improvements in the quality of mask substrates. The substrate is composed of a Low Thermal Expansion Material (LTEM) such as ULE® or Zerodur®, which must have both low average and low spatial variation in thermal expansion. Given the improvements recently made in these materials, they will qualify for use in EUVL substrates. The surface of the substrate is evaluated using three characteristics: roughness, flatness, and number of surface defects. International Sematech and the EUV LLC have funded an effort to purchase substrates as specified by the recently formulated SEMI P37-1101[2] standard in order to assess the capability of commercial vendors as well as to promote further improvement. Even though the SEMI P37 specifications are beyond current capability for fabricating surfaces in high volume, they provide a target for vendors. Measurements of the three metrics are plotted over time and then compared to SEMI P37 in order to assess how well mask substrate fabrication is progressing toward meeting the needs of EUVL.

High reflectivity of the multi-layer coating requires a very smooth substrate. The specified value of high-spatial-frequency roughness of a substrate for EUVL is 0.15 nm RMS. This value has already been achieved for a number of mask substrates made from ULE®, although the majority of substrates, including both ULE® and Zerodur®, fall in the range of 0.2 to 0.4 nm RMS. While some improvement in roughness of the substrate is needed, little risk is associated with achieving the roughness requirement as an independent specification.

The allowable overlay error for EUVL dictates that the mounted mask be very flat, which in turn dictates that the substrate be very flat. Currently, the lowest level of freestanding flatness of LTEM mask substrates is about 0.3 μm PV. This is somewhat better than the best class of quartz substrates widely available for optical lithography, which has flatness of 0.5 μm PV. It is clear that improvements in the final polishing process are required in order to meet the 50 nm P-V that is required for EUVL. However, an improvement in the ability to measure flatness is required first. Due to difficulties in measuring flat parallel-sided substrates, the flatness instruments now installed at the vendors have

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accuracies that are poor compared to SEMI P37 requirements. New-generation instruments are now being developed to accurately measure mask flatness that will enable validation of the SEMI P37 flatness specifications. These new instruments will provide the measurement feedback necessary to further improve the polishing processes that are responsible for substrate flatness.

Surface defects on the substrate propagate through the multi-layer coating if they are greater than a threshold size. For the ITRS 70-nm node, the threshold size is estimated at the equivalent of a 39-nm PSL sphere. This requirement was derived from models of substrate defect printability developed by Gullikson et al.[3] Mirkarimi et al. have shown that the multi-layer coating process can be modified to make up to 50-nm substrate defects not printable.[4] This size is the target in the SEMI P37 standard. Hence, substrate surface defects must be eliminated down to 50 nm size, for which there is currently no method of high-speed inspection. A new defect inspection tool recently demonstrated defect metrology with sensitivity at the 90-nm PSL sphere-equivalent size and at 98% capture probability. While this new capability is providing feedback to the vendors to help them improve their processes, there still remains a gap in size between defects on a substrate surface that can be accommodated and defects that can be detected.

Each of the three independent specifications described above presents substrate vendors with a significant challenge. However, a substrate must simultaneously meet all three specifications in a high-volume manufacturing process and therein may lie the most significant challenge.

2. SEMI STANDARD P37-1101

An early goal in developing and commercializing the technology required to manufacture substrates was to put together a standard that would exactly specify the substrates. The substrate is a highly polished, bare glass slab, onto which various coatings are subsequently deposited and a pattern is written. The SEMI standard, P37-1101 was approved in November 2001 and represents an important step in ensuring the future supply of substrates for EUVL. First, it clearly states the requirements for substrates for EUVL. The requirements target the 45-nm node and are the best collective estimates of a widespread community of mask suppliers, mask users, semiconductor equipment manufacturers, and integrated circuit manufacturers. The specification enables commerce in substrates and allows the fair comparison of results across all potential vendors.

Second, the standard is a consensus document that defines a single target for coordinating the technology development plans of all potential vendors of substrates. The challenge to the commercial infrastructure is to progress from its current capability to produce substrates for optical lithography to a much-improved capability to produce substrates for EUVL.

A summary of the stringent requirements of SEMI P37 is shown in Fig 1. The 152-mm square by 6.35-mm thick bare glass format is the same as currently used for optical lithography and therefore takes advantage of the existing commercial infrastructure for producing mask substrates. The flatness and roughness is tightly controlled over a quality area that excludes a 5-mm border. The high spatial frequency surface roughness (HSFR) over the front-side quality area is to be less than or equal to 0.15 nm Root Mean Square (RMS) and the local surface slope less than or equal to 1 milliradian. The flatness of the front side quality area of the freestanding substrate is specified to be less than or equal to 50 nm Peak-to-Valley (PV), which is a challenging specification for such a thin plate. The flatness requirement in the border region is reduced to 1 μm PV to allow for easier manufacture of the front surface. The flatness of the backside quality area of the substrate is also controlled to be less than or equal to 50 nm PV. This allows for mounting the backside of a mask to an electrostatic chuck in an exposure tool where long spatial wavelength non-flatness of the backside will result in non-flatness of the front side when the substrate is clamped down to the chuck.

Within the front-side quality area, a defect quality area is defined over which no localized light scatterer (i.e., surface defect) greater than 50-nm PSL sphere-equivalent are allowed. Localized light scatterers are any isolated features, such as particles or pits, on or in the substrate surface, resulting in increased light scattering intensity relative to that of the surrounding substrate surface. PSL equivalent size means the detected defect appears to be the same size as a polystyrene latex sphere examined under the same inspection conditions. The defects present on the backside of the substrate are also controlled to be less than 1 μm. This requirement precludes any large defects such as particles from being introduced by the substrate, becoming trapped between the back of the mask and the chuck, and causing a bump

on the front surface as the mask is clamped in an exposure tool. Lastly, the substrate itself is composed of low thermal expansion material (LTEM) falling into one of four classes over the temperature range from 19 °C to 25 °C. The lowest grade of material, "Class D," must have an average coefficient within ±30 x 10^{-9}/K and a spatial variation within a substrate of less than or equal to 10 x 10^{-9}/K. The highest grade of material, "Class A," must have an average coefficient within ±5 x 10^{-9}/K and a spatial variation within a substrate of less than or equal to 6 x 10^{-9}/K.

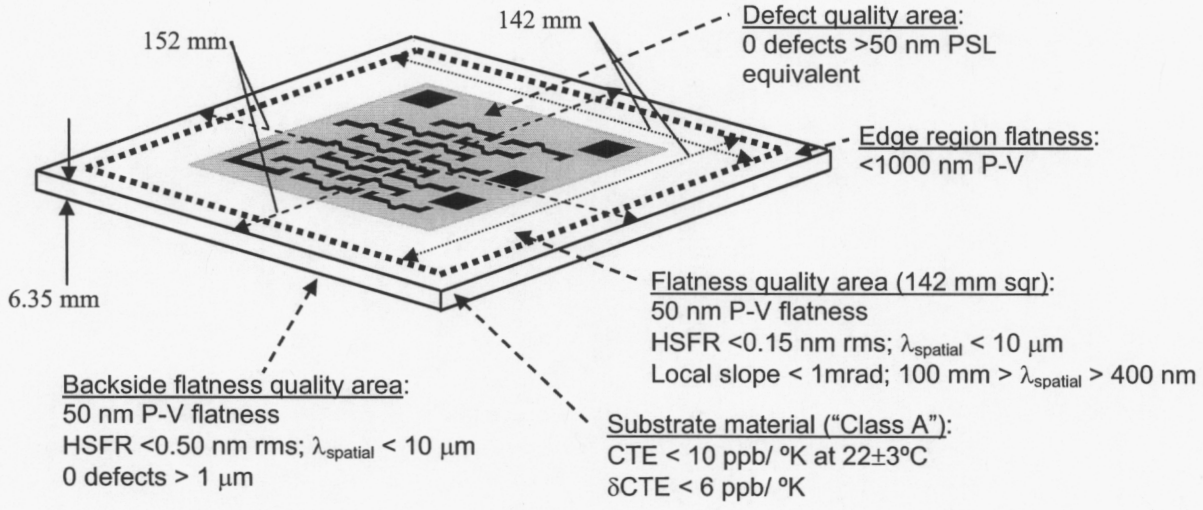

Fig. 1: Excerpt from SEMI P37-1101 substrate requirements

3. MATERIAL

A contributor to Image Placement Error (IPE) at the wafer is the in-plane distortion (IPD) of the patterned mask that arises from its temperature being different during exposure from that at which it was written and inspected. The change in the temperature of the mask from writing to exposure comprises both a change in its average temperature and the spatial variation about its average. The change in the temperature may be induced, for example, by a difference in temperature of the environment or by the energy absorbed as the mask is scanned during EUV exposure.[5,6]

In-plane distortion results from the interaction of the change in the temperature of the mask and the coefficient of thermal expansion of the mask. Again, the coefficient of thermal expansion of the material comprises both the average value plus the spatial variation about the average. Because uniform dilation of the mask is routinely compensated in lithography by changing magnification during exposure, it is only the remaining in-plane distortion about the average that is not compensable and is of interest here. It is useful to partition the non-compensable distortion into that which results from a change in average temperature and that that results from a temperature gradient. Such a partition leads to the conclusion that the mask substrate must have a small average thermal expansion in order to control the non-compensable distortion due to a temperature gradient and the need for a small variation in thermal expansion in order to control the non-compensable distortion due to a change in average temperature.

The two leading candidate materials are ULE® and Zerodur®. ULE is an amorphous silica (SiO_2) glass containing about 7.5 mol % titania (TiO_2). The Ti atoms substitute the Si atoms and form a solid solution rather than forming a separate phase if the titania content is kept below ~10 mol%. It can be polished to very low roughness as shown in Fig. 2, which is an AFM image of a typical substrate surface. This ULE surface meets the roughness requirements of SEMI P37. Currently available ULE falls within Class D with an average thermal expansion (CTE) in the range ±30 x 10^{-9}/K, although it suffers from spatial variation in the CTE of about 20 x 10^{-9}/K within a single boule of material. However, substrates can be taken from the boule to minimize the spatial variation of the patterned surface of a substrate. These values are all determined by using samples of 100-mm length, and hence the magnitude of CTE spatial variation could

be different for different gage lengths. According to Corning, its manufacturer[7], the quality of ULE has recently been improved, particularly with regard to its homogeneity, to qualify for SEMI P-37 "Class A" material.

Zerodur is a two-phase material comprising approximately 75% crystalline phase and 25% glass phase. The thermal expansion is negative for the crystal phase and positive for the glass phase. The overall thermal expansion can be adjusted by controlled thermal treatment during manufacture. Zerodur can also be polished to very low roughness on small samples, but requires further polishing development to meet the specification for EUVL substrates. A typical AFM image of a substrate surface is also shown in Fig 2. Currently available Zerodur falls close to Class C material with an average thermal expansion in the range $\pm 15 \times 10^{-9}/K$ and spatial variation of about $12 \times 10^{-9}/K$[8]. These values are also determined by using samples of 100-mm length and hence the magnitude of CTE spatial variation could be different for different gage lengths. Zerodur has also recently been improved to qualify for "Class A" material according to Schott Glas, its manufacturer[9].

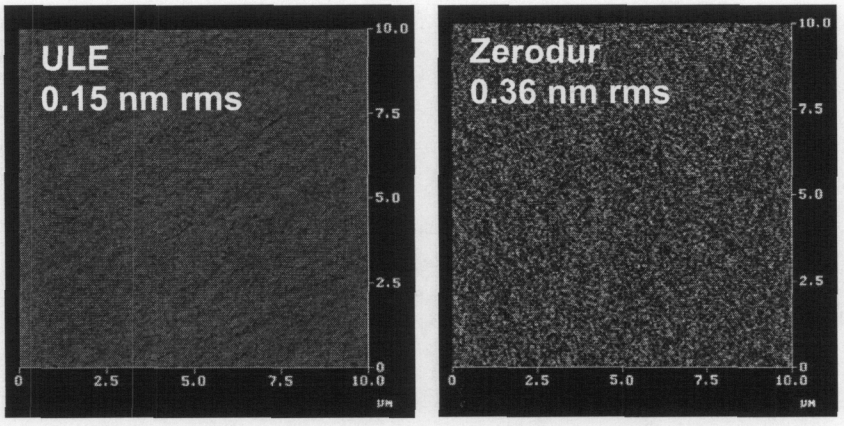

Fig. 2: Images from polished substrate surfaces of ULE (left) and Zerodur (right)

The requirements stated in SEMI P37 are currently beyond our ability to measure. First, the uncertainty of determining the average CTE over the range of 19 °C to 25 °C is about the same magnitude as the specified value itself for "Class A" material. Second, CTE measurements, which are made over gage-lengths of 100mm, are insensitive to, for example, a sinusoidal spatial variation of 100 mm wavelength. New instrumentation is being proposed to allow better measurement of both average CTE and spatial variation in CTE.

It is worth noting that the mask is treated here as though it were freestanding or unconstrained in the plane of its patterned surface as it is mounted in, for example, a lithographic exposure tool. This will likely not be the case for EUV Lithography. In the current designs for chucks to hold the masks during exposure, the mask is electrostatically attracted to a planar surface in order to "flatten" the mask. The mask becomes constrained by the chuck from thermally growing in the plane of the pattern by friction between the mask and chuck. Martin et al. have modeled this case, which clearly shows that the specification of thermal expansion of the substrate material should take into account that the mask and its chuck are a system.[10]

4. ROUGHNESS

For EUVL, a multi-layer coating is deposited onto the substrate to attain high reflectivity at 13.4-nm wavelength. Achieving high reflectivity requires a very smooth substrate as shown in Fig 3, which shows how reflectance degrades as the substrate surface becomes rougher. The specified value of high-spatial-frequency roughness of a substrate for EUVL is 0.15 nm RMS and represents a compromise between reflectance and difficulty to polish the surface.

Batches of substrates have been periodically purchased over the past two years in order to evaluate commercial vendors' ability to achieve the required roughness specification. Sample roughness measurements are made from each of the

delivered batches, usually of five or ten substrates. The roughness is measured using an Atomic Force Microscope over 1-μm and a 10-μm square scans. Also, measurements are made at the center and toward the edge of the substrate, because uniform roughness across a substrate is required in addition to low roughness. If roughness varies across a substrate, then the concomitant change in reflectivity will result in a change in the dose at the wafer making it difficult to control printed line-width.

The average roughness per batch of ULE substrates is shown in Fig 4 for three different commercial vendors. Within the results from each vendor, the older measurements are to the left and newer measurements to the right, but the time periods from one batch to the next are not equal. For vendor A, there has clearly been improvement with time. For vendor B, the variation over time is about the same as the variation within the batches, which tend to be fairly consistent. As can be seen, the majority of measurements fall in the range of 0.2 to 0.4 nm RMS, although vendor B has already achieved the specified value of 0.15 nm RMS.

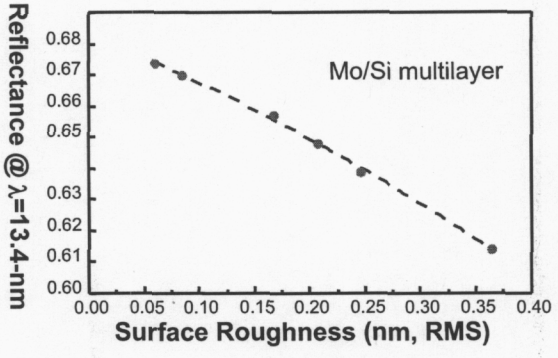

Fig. 3: Reflectance at EUV degrades with increasing substrate surface roughness [11]

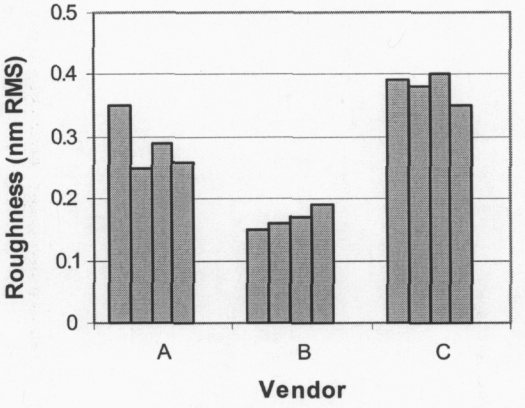

Fig. 4: Average roughness per batch of ULE substrates for three different vendors

In general, while some improvement in roughness of the substrate is needed, little risk is associated with achieving the roughness requirement as an independent specification. Small samples of both ULE and Zerodur have been polished to sub-Angstrom roughness, so there is no question that these materials can be polished to the SEMI P37 specification. The remaining task is to scale up the polishing processes to accommodate the large surface of a mask substrate and in production quantity.

5. FLATNESS

The allowable overlay error for EUVL dictates that a patterned mask be mounted very flat in the exposure tool. The need for mounted flatness stems from current EUV imaging system designs, which call for non-telecentric illumination of the mask as shown in Fig 5. Here, the consequence of non-telecentricity is that an error in the placement of the image occurs at the wafer for a variation in the height of the patterned mask surface (i.e., the non-flatness). The image placement error at the wafer is about one-fortieth of the non-flatness of the mounted mask at the nominal 5-degree illumination angle shown. A fraction of the allowable overlay error is attributed to as-mounted mask front surface flatness. This is then further apportioned over a number of contributors, one of which is the freestanding flatness of the substrate, and which SEMI P37 currently specifies at 50 nm PV. In addition, because a flat-faced, electrostatic chuck is currently the designated method of mounting a mask in an exposure tool, the flatness of the backside of the mask must also be controlled. This is because non-flatness of the backside influences the non-flatness of the patterned side as the mask is clamped against the chuck. Again, SEMI P37 allows 50 nm PV non-flatness of the backside of a freestanding substrate. SEMI P37 does not assume that the chuck flattens the substrate. This assumption is probably correct for short spatial wavelength substrate non-flatness such as "ripple." This is a very conservative assumption for long spatial wavelength substrate non-flatness such as "bow." A SEMI standard for mask chucking is being discussed. If such a standard is

established, then the flatness requirements in the substrate standard might be changed to permit certain types of flatness error (e.g., bow) that might be compensated by chucking.

Batches of substrates have been periodically purchased over the past two years in order to evaluate commercial vendors' ability to achieve the required specification of 50 nm PV. Sample flatness measurements of the front side of the substrate are made from each of the delivered batches. The flatness of the front side of a substrate is measured using a general-purpose interferometer by spoiling the backside reflection with an antireflection coating. While this measurement is adequate for tracking vendor progress in the early stages of improvement, it has two shortcomings. This method of flatness measurement is destructive in that it introduces defects associated with the coating and handling procedures. Also, front side flatness is only one of the flatness measurements required by SEMI P37, which also specifies backside flatness and thickness variation.

The front-side flatness measurements taken to date are shown in Fig 6. Again, the older measurements are to the left and newer measurements to the right within a single vendor, but the period in time from one batch to the next varies. Figure 6 demonstrates that significant improvement in flatness has been achieved at two of the vendors. The lowest level of freestanding flatness of LTEM mask substrates is about 0.3 μm PV. This is somewhat better than the best class of quartz substrates used in optical lithography, but it is quite far from the target value of SEMI P37 of 50 nm. The flatness values plotted are average values for a batch, but this is somewhat misleading because, in contrast to the roughness measurements, the flatness measurements vary significantly within a batch of substrates.

It is clear that further improvements to the final polishing process are required in order to meet the 50 nm PV flatness that is required for EUVL. However, improvement in the ability to measure flatness is required first. Due to difficulties in interferometrically measuring flat, parallel-sided substrates, the flatness instruments now installed at the vendors have accuracies that are poor compared to SEMI P37 requirements. New-generation instruments are now being developed to accurately measure mask flatness that will enable validation of the SEMI P37 flatness specifications. These new instruments will provide feedback to enable the development of improved polishing processes.

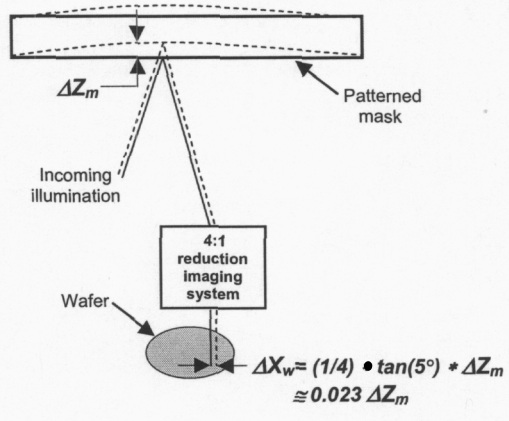

Fig. 5: Non-telecentric illumination results in an image placement error at the wafer for a flatness error of the mask as it is mounted in an exposure tool

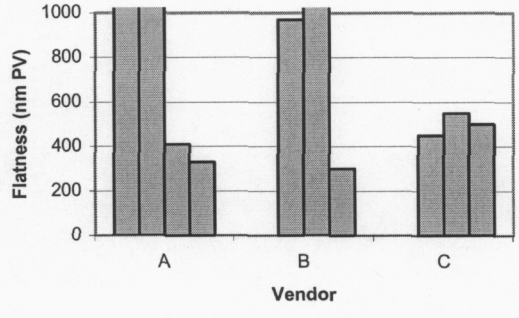

Fig. 6: Front surface flatness averaged over each batch

6. SURFACE DEFECTS

Surface defects on a substrate propagate through the multi-layer coating, and if they are greater than a threshold size can appear as defects in the image that is produced at the wafer. Figure 7 shows a Transmission Electron Microscope photomicrograph of the cross-section through a reflective Mo/Si multi-layer deposited over a 60-nm gold sphere on the surface of a substrate. The multi-layer tends to smooth over the defect, but the perturbation to the reflected wavefront can still make the defect print at the wafer. For the ITRS 70-nm node, the threshold size is estimated at the equivalent of

a 55-nm PSL sphere. Hence, SEMI P37 specifies that there be no substrate surface defects greater than 50-nm PSL sphere-equivalent. Another perspective on allowable defect levels comes from a cost-of-ownership model for masks[12], which concludes that defect levels on the substrate before coating, again at the 50-nm size, should be less than about 0.0025 defects per square centimeter. The latter defect density value is used here to track progress of the vendors.

There is no inspection tool for the detection of 50-nm defects on a bare glass surface. However, a prototype tool[13] has demonstrated defect detection with sensitivity at the 90-nm PSL sphere-equivalent size at 98% capture probability. Although this tool is not fully capable of inspecting substrates to assess whether they are SEMI P37 compliant, it can provide valuable information with which to track progress and for feedback to the vendors. Figure 8 shows the results of measurements made on vendor-supplied LTEM substrates. Unlike the roughness and flatness histograms where batch-averages are plotted, single substrate measurements are plotted for the histogram of defect density.

Three observations arise from Fig 8. The first is that the defect levels span three orders of magnitude from 0.05 to 50 defects/cm^2. Even within a single vendor, defect levels are quite inconsistent from substrate to substrate. For example, the two recent measurements from Vendor A differ by more than an order of magnitude. We have yet to determine the causes of the variation, which stands in stark contrast to the very consistent roughness measurements. The substrates are shipped from the vendor and a pellicle is mounted on the substrates to protect them during inspection and associated handling. Therefore, some of the defects detected may have been added during shipping and handling. The second observation is that polishing processes are capable of producing surfaces with 0.05 defects/cm^2. Inspections at this level were observed in two different batches of substrates manufactured more than a year apart. This is quite far from the target value of 0.0025 defects/cm^2 at 50-nm sensitivity but is at about the same level as the defects currently added during the deposition of the reflective multi-layers[14]. The third observation is that there is no trend of decreasing defect levels with time to indicate that learning is occurring such that over time, defects levels will diminish to the value required by EUVL. Again, this contrasts with the improving trend of the average flatness measurements. These three observations lead to the conclusion that significant acceleration is needed in the reduction of defect levels on substrates.

Figure 8 indicates the need for further defect inspections in a well-designed experiment to determine the causes of the small defects. A first step is to use alternative methods such as Atomic Force Microscopy to fully characterize the defects that are currently detected by the prototype tool. In the future 50-nm PSL-equivalent sensitivity will be needed in order to fully support the 70-nm node, with a further sensitivity improvement to 32 nm needed to support the 45-nm node.

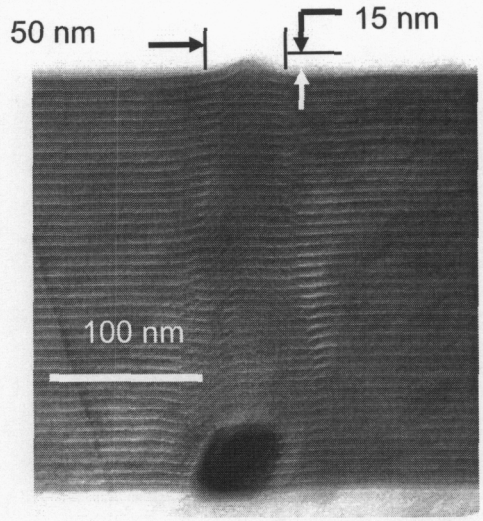

Fig. 7: A defect on the surface of the substrate is smoothed over by the multi-layer, but causes a significant perturbation to the reflected wavefront[15]

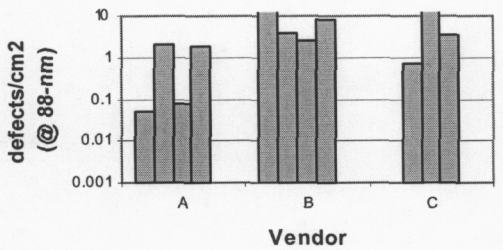

Fig. 8: Aerial density of defects larger than 90-nm PSL sphere-equivalent on LTEM substrates

7. METROLOGY

Evaluating mask substrates has been made difficult by the shortage of accurate flatness measuring tools and sensitive defect inspection equipment, which is an impediment to improving the finishing processes required to support EUVL. Two significant advances have been made in these areas. First, laboratory demonstrations have been made and commercial flatness measuring interferometers are now being introduced that can make nondestructive front-side and backside flatness measurements and thickness variation measurements on a substrate to the accuracy required by SEMI P37. Second, a prototype photomask pattern defect inspection tool has been applied to unpatterned substrate defect inspection and shown to have a sensitivity of 90-nm PSL-equivalent size.

The preferred interferometer employed by most of the substrate vendors uses grazing incidence, which can separate the measurement of flatness of the front and rear surfaces of a bare glass substrate. However, this type of interferometer suffers from poor accuracy and cannot be extended to the accuracy required for inspecting EUVL substrates. Grazing incidence is used because conventional interferometric testing of the front-side and backside flatness of a "window", that is, a parallel-sided bare glass substrate, has been difficult because of the long coherence length of the HeNe lasers that have typically been used as sources for these phase-measuring interferometers. The long coherence length confounds the interference fringes from both surfaces and does not allow the separate determination of the individual surface flatnesses. Although we have been using such a general-purpose interferometer to make measurements, we must apply an antireflective coating to the backside of the substrate in order to measure the individual flatness of the front surface of the substrates. The application and removal of the antireflective coating subjects the backside to damage in the form of added defects.

There are a number of methods that can be used to separate front and back surface flatness[16]. One approach to measuring EUVL substrates was demonstrated at the National Institute for Standards and Technology (NIST) using a conventional HeNe phase-shifting interferometer in a Ritchey-Common configuration[17]. Also, commercial instruments that can make accurate measurements of EUVL substrates are just becoming available. One such instrument is based on Fourier Transform Phase-Shifting Interferometry described by L L Deck[18]. A different approach was demonstrated at Lawrence Livermore National Laboratory (LLNL) using a short-coherence length laser in a Fizeau configuration. Here, the phase shifting diffraction interferometer[19] developed for the EUVL Program was used as the source. It has two distinct properties that eliminate the multiple beam interference and permit selective interference between only one substrate surface and a reference flat: (1) a short coherence length; (2) the ability to adjust the time delay between the interfering beams so that only the pair of interest are temporally coherent.

In this setup, three measurements (M_1, M_2, and M_3) are made as shown in the setup in Fig 9. The substrate is interposed between a reference transmission flat and a reference mirror for all three measurements without any repositioning. The coherence length, which is about 2 mm, must be significantly less than the optical path length between the front and rear surfaces of the substrate, which is about 9 mm. The adjustable delay between the two beams determines which two surfaces are interfered in the three measurements. From the three measurements, the flatness of side A and side B, the thickness variation, and the variation in index of refraction are calculated respectively as:

$\underline{S}_A(x,y) = M_1(x,y)/2$

$\underline{S}_B(x,y) = M_2(x,y)/2$

$\underline{t}_S(x,y) \bmod(\lambda) = [M_1(x,y) + M_2(x,y)]/2$

$\underline{n}(x,y) = M_3(x,y) / [M_1(x,y) + M_2(x,y)]$.

The accuracy of these measurements depends on knowledge of the reference flats, which must be characterized and this information used to correct the three measurements. The calibration of the reference flats is one of the limiting errors in this interferometer.

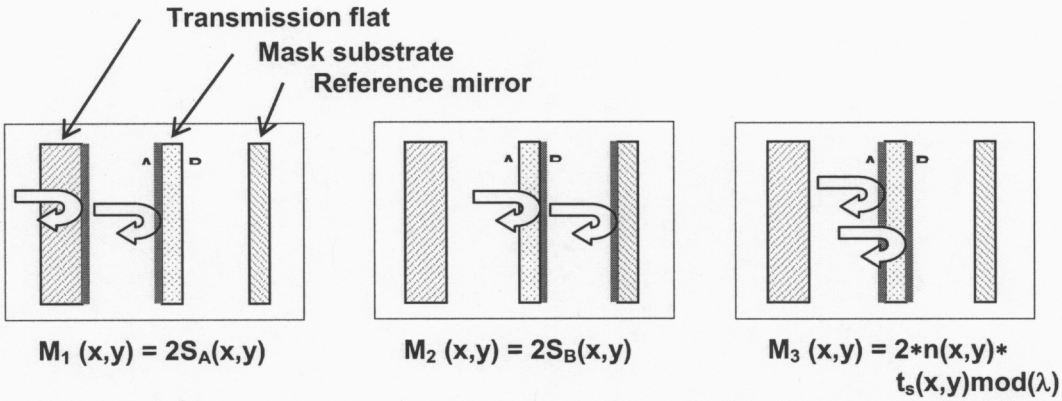

Fig. 9: A Fizeau interferometer that uses a short coherence source allows the independent determination of flatness of the front and back surfaces, the thickness variation and the variation in refractive index from three measurements: M_1, M_2, and M_3

A demonstration measurement was made using the basic configuration described above. The results are shown in Fig 10 for the central 4-inch area of a substrate. The gray-scale shows that the substrate is dished and is thicker at two edges than at the center. In addition, there is a slowly varying change in the index of refraction, which is displayed as an equivalent variation in optical path length over the thickness of the substrate. Based on this demonstration measurement, an interferometer is being built that is capable of full-size acceptance testing of EUVL substrates. It will be used for feedback to substrate vendors as well as making comparative flatness measurements as the vendors bring improved interferometry on line, which needs to be qualified by independent means.

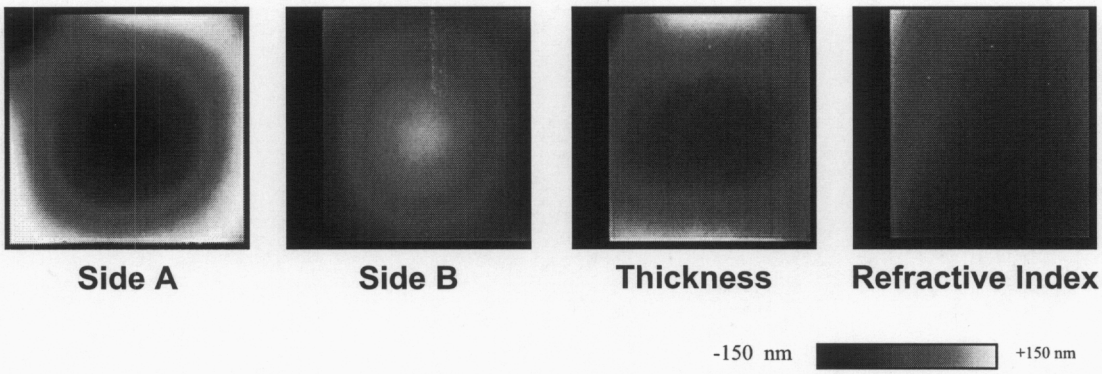

Fig. 10: A demonstration measurement of a substrate shows the independent measure of front and back surface flatness, the variation in thickness and the variation in refractive index

A second advance in metrology has been made in the detection of small defects on the surface of an EUVL substrate. A prototype mask pattern defect inspection tool has been qualified to perform unpatterned substrate defect inspection at a sensitivity of 90-nm PSL-equivalent size. The development of the inspection tool itself was sponsored in part by NIST-ATP under a KLA-Tencor Cooperative Agreement[20]. To extend the use of the tool to inspecting unpatterned substrates, a "calibration" substrate was fabricated to determine the sensitivity of the tool in detecting small defects on a bare glass substrate. It was prepared by depositing regions of uniformly sized PSL spheres on ULE, one of the candidate low thermal expansion substrate materials. The sphere sizes were 65 nm, 77 nm, 88 nm, 101 nm and 126 nm. The aerial density of the deposited spheres was about 200 per square centimeter.

Figure 11 shows the tool's user-interface screen for the calibration substrate. A qualitative feel for the tool's sensitivity is seen in that a high density of spheres is detected in the clumps containing larger PSL spheres of 126-nm (at 5 O'clock),

101 nm (at 1 O'clock) and 88 nm (at 11 O'clock). A low density of spheres is detected in the clumps containing smaller PSL spheres of 77 nm (at 7 O'clock) and 65 nm in the center. The actual probabilities of detection were obtained by repeatedly inspecting a small areas of a calibration mask with known size of PSL spheres. The mean number of detected defects and the variance are then used to infer the probability of detection, which is assumed to be binomially distributed. The calibration mask showed that 88-nm PSL spheres were detected at greater than 97% confidence on the bare ULE surface.

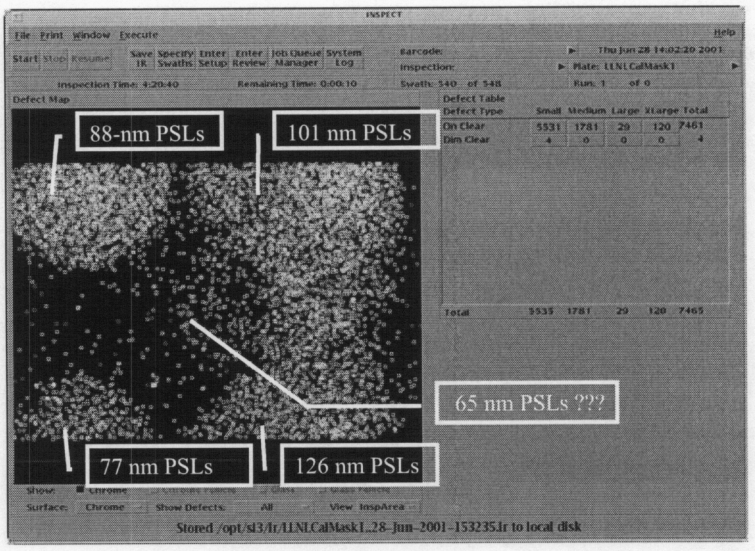

Fig. 11: Output screen from inspection tool showing defect calibration substrate

As mentioned earlier, the 70-nm node requires that defects on the substrate be detected at the size equivalent of a 50-nm PSL sphere, which indicates a need for further sensitivity improvements for unpatterned inspection. However, this new capability at 90-nm sensitivity is providing feedback to the vendors to help them improve their processes.

8. SUMMARY AND CONCLUSIONS

Developing manufacturing infrastructure is required to ensure a commercial source of EUVL mask substrates in time for EUVL. A number of accomplishments have already been made. The substrate has been exactly specified in SEMI standard P37. Two material suppliers are routinely producing low thermal expansion material and that is being improved to meet the highest class designated in SEMI P37. New measurement tools are becoming available for evaluating the characteristics specified in SEMI P37. Three vendors have been finishing substrates for evaluation on a regular basis and have roadmaps in place for meeting the specifications of SEMI P37.

We have been evaluating three challenging metrics to determine the state of the infrastructure for the finishing substrates. First, surface roughness is on track and while some improvement is needed, little risk is associated with achieving the roughness requirement as an independent specification. Second, with new flatness-measuring equipment just coming on line, the vendors are poised for improvement toward the SEMI P37 specification. Third, significant acceleration is needed in the reduction of defect levels on substrates. The lack of commercially available defect metrology is limiting progress in developing substrates for EUVL. Hence, one of our goals is to get on a defect reduction learning curve that leads to the target defect density for EUVL mask substrates, which will require both better availability of defect measuring tools and accumulating cycles of learning of the vendors.

Each of the three independent metrics described above presents substrate vendors with a significant challenge. However, a substrate must simultaneously meet all three metrics in an economic high-volume manufacture process. Therein may lie the most significant challenge. Each finishing vendor has a key R&D effort to develop polishing processes for

producing a flat, ripple-free, smooth substrate surface. To reduce the risk associated with this challenge, alternative methods to ensure that substrates can meet the needs of EUVL are also being pursued. For example, if an electrostatic chuck becomes the prescribed method for mounting a mask, then it can be relied upon to remove some of the low-order substrate non-flatness. Also, on-going research on ion-beam deposition shows that smoothing of the substrate surface occurs prior to the deposition of the reflective multiplayer. Together, these two efforts hold potential for relaxing the roughness requirement and the low-order flatness requirement of the substrate surface. The result would be a less expensive, easier-to-manufacture substrate.

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